The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A pixel sensor cell comprising:

a pinned photodiode;

a transfer transistor placed between the pinned photodiode and an output node, the transfer transistor being a depletion mode MOSFET;

a reset transistor coupled between a high voltage rail V_{dd} and the output node; and

an output transistor, the gate of the output transistor being coupled to the output node.

2. The pixel sensor cell of Claim 1 further including a row select transistor, the gate of the row select transistor being coupled to a row select line, the input of the row select transistor being coupled to the output of the output transistor, and the output of the row select transistor providing the output of the pixel sensor cell.

3. The pixel sensor cell of Claim 1, wherein the output node is the source of the transfer transistor and said pinned photodiode is the drain of said transfer transistor.

4. The pixel sensor cell of Claim 1, further including a negative voltage generator that generates a negative voltage sufficient to turn off said depletion mode transfer transistor.

5. The pixel sensor cell of Claim 1, wherein said depletion mode transfer transistor has a threshold voltage near V_{dd}.

6. The pixel sensor cell of Claim 1, wherein said depletion mode transfer transistor has a threshold voltage of substantially -0.9 volts or less.

7. The pixel sensor cell of Claim 1, wherein the pinned photodiode is a P+/Nwell/Psub structure and said transfer transistor is an N-type MOSFET.

8. The pixel sensor cell of Claim 1, wherein the pinned photodiode is a N+/Pwell/Nsub structure and said transfer transistor is a P-type MOSFET.

9. A CMOS image sensor comprising:

a plurality of active pixels arranged in rows and columns, at least one of said active pixels comprising:

(a) a pinned photodiode;

(b) a transfer transistor placed between the pinned photodiode and an output node, the transfer transistor being a depletion mode MOSFET; and

(c) a reset transistor coupled between a high voltage rail V_{dd} and the output node; and

(d) an output transistor, the gate of the output transistor being coupled to the output node.;

a processing circuit for receiving the output of said active pixels; and

an I/O circuit for outputting the output of said active pixels off of said CMOS image sensor.

10. The image sensor of Claim 9 further wherein said active pixel includes a row select transistor, the gate of the row select transistor being coupled to a row select line, the input of the row select transistor being coupled to the output of the output transistor, and the output of the row select transistor providing the output of the pixel sensor cell.

11. The image sensor of Claim 9, wherein the output node is the source of the transfer transistor and said pinned photodiode is the drain of said transfer transistor.

12. The image sensor Claim 9, further including a negative voltage generator that generates a negative voltage sufficient to turn off said depletion mode transfer transistor.

13. The image sensor of Claim 9, wherein said depletion mode transfer transistor has a threshold voltage near V_{dd}.

14. The image sensor of Claim 9, wherein said depletion mode transfer transistor has a threshold voltage of substantially -0.9 or less volts.

15. The image sensor of Claim 9, wherein the pinned photodiode is a P+/Nwell/Psub structure and said transfer transistor is an N-type MOSFET.

16. The image sensor of Claim 9, wherein the pinned photodiode is a N+/Pwell/Nsub structure and said transfer transistor is a P-type MOSFET.

17. An active pixel for use in a CMOS image sensor, the active pixel including a pinned photodiode, a depletion mode transfer transistor that selectively transfers charge from the pinned photodiode to an output node, and a reset transistor couple to the output node to reset the output node to a reset voltage during a reset period.

18. The active pixel of Claim 17, further including a negative voltage generator that generates a negative voltage sufficient to turn off said depletion mode transfer transistor.

19. The active pixel of Claim 17, wherein said depletion mode transfer transistor has a threshold voltage near V_{dd}.

20. The active pixel of Claim 17, wherein the pinned photodiode is a P+/Nwell/Psub structure and said transfer transistor is an N-type MOSFET.